Q.2 a. How integrated resistors are fabricated? Explain diffused resistor method in detail?

Answer:

ANS 2(a) The basic technique for obtaining a resistor in integrated circuit is by utilising the bulk resistance of a defined volume of semiconductor region.

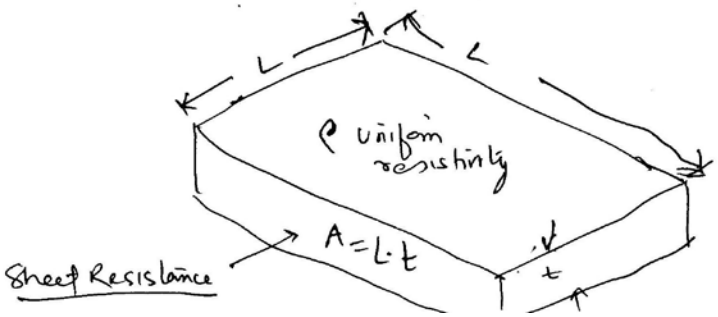
Diffused Resistor: In this method, resistor is formed in one of the isolated regions of epitaxial layer during base or emitter diffusion common to bipolar transistor fabrication. This type of resistor is very economical. The value of the resistance depends upon the surface geometry. That is, length, width and upon the diffused impurity profile. In this context, a very useful quantity sheet resistance is defined as diffused layers are very thin. The resistance of the sheet of material can be written as

$$R_S = \frac{\rho L}{Lt} = \frac{\rho}{t}$$

Consider the square L×L of a material of resistivity ρ, thickness t, and cross sectional area A = L×t shown in fig. The resistance of these resistors can be expressed in terms of the sheet resistance R_S and surface dimensions L and W

$$R = \rho \frac{L}{Wt}$$

where ratio L/W is called the aspect ratio of the surface geometry and is, therefore, the effective number of square contained in the resistor.



therefore the effective number of square contained in the resistor: the base resistor in the range of 20Ω to 30 kΩ can be easily fabricated due to medium resistivity p type base region

b. Why aluminium is usually used for metallization of most ICs?

Answer:

(b) (i) It is relatively a good conductor
(ii) It is easy to deposit aluminium films using vacuum deposition
(iii) Aluminium make good mechanical bonds with silicon
(iv) Aluminium forms low resistance, non-rectifying contact with p type silicon and the heavily doped n type silicon

c. Explain the self aligning property of a polysilicon gate MOSFET

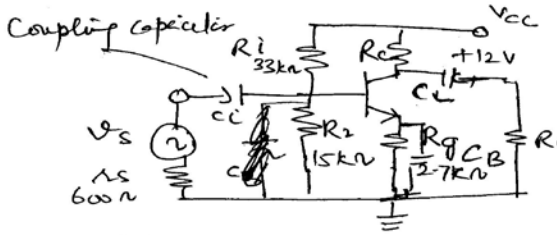
Answer:

(c) The polysilicon-gate provides self alignment of the gate with the source and drain. In the conventional metal gate structure, the gate electrode is normally designed to overlap the edges of the source and drain region by about 5 μm to avoid any masking errors. This, however, results in small overlap capacitance C_{gs} between gate G and source S and C_{gd} between gate G and drain D. These capacitances are of order of 1 to 3 pF and lower the speed of operation and increases the power consumption. The silicon gate due to self aligning property eliminates these capacitances

Q.3 a. Explain the need for coupling and bypass capacitors in transistor circuits, and draw AC Equivalent circuit of CE amplifier.

Answer:

Ans: 3 The capacitor C_i is used to couple the signal source to the circuit input. Because C_i is an open circuit to direct current, V_s does not affect the level of V_B. Capacitor C_i behave as a short circuit for the ac signal V_s, so that the signal voltage (V_s) appears at the transistor base as shown in fig. In this case the signal is said to be ac coupled to the circuit input and C_i is

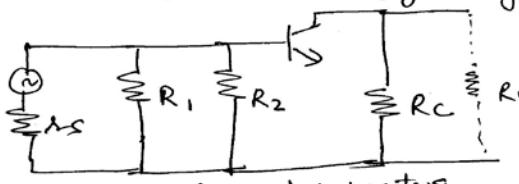


referred to as a coupling capacitor. Input coupling capacitors are normally used with all types of base circuits, otherwise the circuit bias conditions will be altered. Due to coupling capacitor the supply voltage at the transistor collector terminal is reduced from V_{cc} to $V = \frac{V_{cc} * R_L}{R_c + R_L}$ and the collector resistance becomes

$R = R_c \| R_L$

This has the effect of altering the circuit dc load line and Q point. The capacitor C_B offers a short circuit to ac signals so that there is no feedback from the transistor collector to the base. When C_B is replaced with a short-circuit, R_{B_1} and R_{B_2} appear in parallel with the circuit input and output respectively. Second problem of ac degeneration is eliminated by the emitter bypass capacitor C_E

AC Equivalent Circuit : Capacitors behave as short circuits to ac signals so in the ac equivalent circuit for a transistor circuit all capacitors must be replaced with short circuits because the dc supply voltage is not affected by the ac signals. Also all power supplies have large value capacitors at the output terminals, and these will offer shorts circuits to ac signals. Substituting short circuits in place of all the power supply and all capacitors in the circuit below fig gives ac equivalent circuit



Power supply and capacitors behave as ac short-circuits

. If R_L is present, it appears in parallel with R_c in the ac equivalent circuit

b. Use the simplified h-parameter model to derive equations for the current gain A_i, the input impedance R_{in}, the gain A_v and the output impedance R_{out} for the emitter follower circuit shown in Fig.2. Calculate the value of these parameters, assuming h_{ie}= 1100Ω , R_e = 10 KΩ , h_{fe} = 50 and R_s = 1kΩ

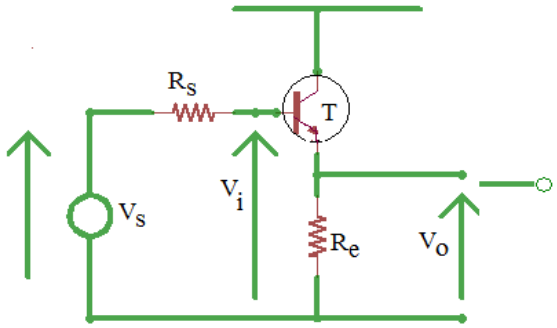
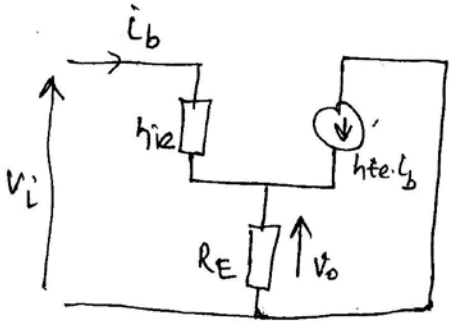


Fig.2

Answer:

3b Equivalent circuit & diagram is



$$A_V = \frac{V_o}{V_i} \approx \frac{h_{fe} i_b R_E}{h_{ie} i_b + R_E h_{fe} i_b}$$

$$= \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E} = 1 - \frac{h_{ie}}{R'_{in}}$$

$$R_{in} = \frac{v_i}{i_b} \approx \frac{h_{ie} i_b + h_{fe} i_b R_E}{i_b} = h_{ie} + h_{fe} R_E \approx h_{fe} R_E$$

$$R_{out} = \frac{V_o(oc)}{i_o(sc)} = \frac{i_b (R_s + h_{ie})}{h_{fe} i_b} = \frac{R_s + h_{ie}}{h_{fe}} =$$

$A_i \simeq 50$ $\quad R_{in} = 1.1\,k\Omega + 50 \times 10\,k\Omega \simeq 500\,k\Omega$

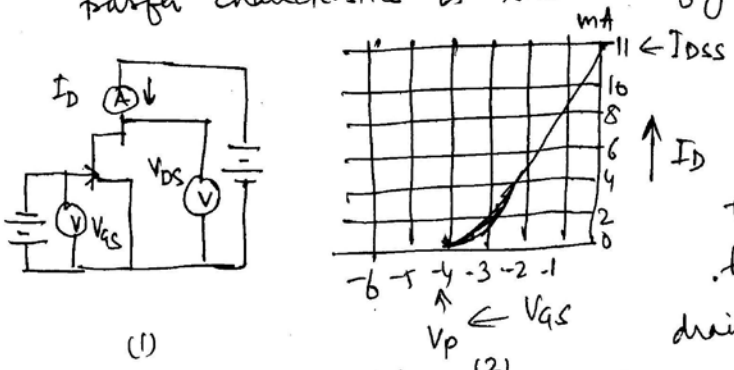
$A_V = 1 - \frac{1100}{50 \times 10^3} = 0.98$ $\quad R_{out} = \frac{1k\Omega + 1.1k\Omega}{50} = 42\Omega$

$R'_{out} = R_{out} \parallel R_E = 10k\Omega \parallel 42\Omega = 42\Omega$

Q.4 a. Draw and explain the transfer characteristics of JFET. List the advantages of JFET.

Answer:

4a The transfer characteristics for an n channel JFET are a plot of I_D versus V_{GS}. The gate source voltage of a FET controls the level of the drain current, so the transfer characteristics is shown in fig.



The transfer characteristics extends from $I_D = I_{DSS}$ at $V_{GS} = 0$ to $I_D = 0$ at $V_{GS} = V_P$. fig 1 shows that the drain-source voltage is maintained constant, V_{GS} is adjusted in convenient step and corresponding level of V_{GS} and I_D are recorded. The characteristics shows that as $-V_{GS}$ is increased I_D is progressively reduced from I_{DSS} at $V_{GS} = 0$ to $I_D = 0$ at $V_{GS} = -V_P$. The transfer characteristic for a FET can be derived from the drain characteristics. A line is drawn vertically on the drain characteristics to represent a constant V_{DS} level

b. The constant current circuit shown in Fig.3 uses a JFET whose operation is described by the equation

$I_D = I_{DSS}(1-V_{GS}/V_P)^2$, $I_{DSS} = 8$ mA and $V_p = 4$ V

(i) Draw the equivalent circuit as an amplifier

(ii) Calculate the required value of R to give a current of 0.5 mA

(iii) If the FET drain- source resistance r_{ds} is equal to 50 KΩ at I_D =0.5 mA, determine the incremental resistance of the circuit for the value of R calculated in (ii)

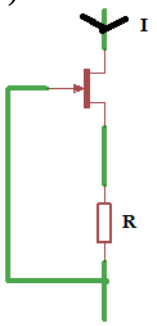
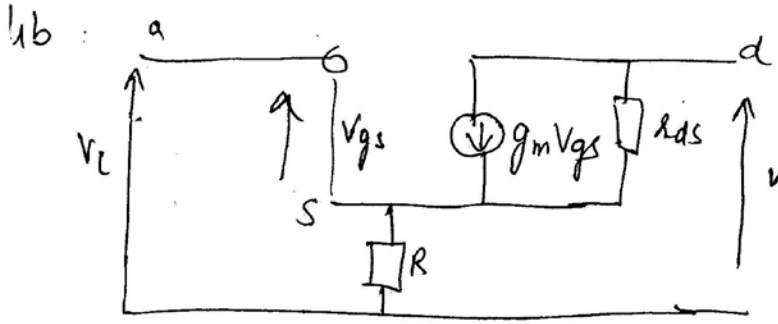


Fig.3

Answer:

4b :



equivalent circuit as an amplifier

(ii) from the equation for I_D

$0.5 \times 10^{-3} = 8 \times 10^{-3} \left(1 + \frac{V_{GS}}{4}\right)^2 \quad \therefore \quad V_{GS} = -3V$

But $R = \frac{-V_{GS}}{I_D} = \frac{3V}{0.5\,mA} = 6\,k\Omega$

(iii) The output resistance is found from $R_o = \frac{v_o(oc)}{i_o(sc)}$

with output open circuit $v_o(oc) = -g_m v_i r_{ds}$

with output short circuit

$V_{gs} = v_i + R i_{(sc)}$ But $i_o(s) = \frac{-g_m V_{gs} r_{ds}}{R + r_{ds}}$

$i_o(sc) = \frac{-g_m r_{ds}}{R + r_{ds}} (v_i + R i_o(sc))$

$i_o(sc) = \frac{g_m r_{ds} v_i}{R + (1 + g_m R) r_{ds}} = \frac{v_o(oc)}{i_o(sc)} = R + (1 + g_m R) r_{ds}$

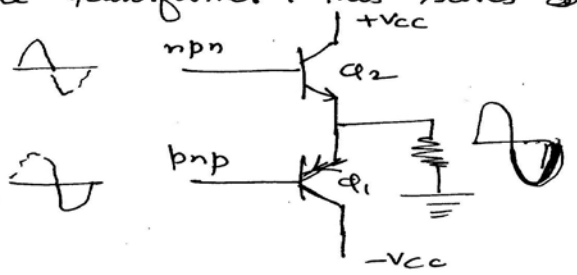
$= 356\,k\Omega$

Q.5 a. Draw and explain the circuit of complementary emitter follower.

Answer:

Two BJTs connected to function as emitter follower whereas one is npn and other is pnp, the devices are selected to have similes parameters, so they are complementary transistors. The circuit is termed as a complementary emitter follower. A complementary emitter follower have similar signal applied simultaneously to both device bases as shown in fig. Transistor Q_1 conducts during the positive half cycle of the signal and it pulls the output voltage up to follow the input. During this time Q_2 base-emitter

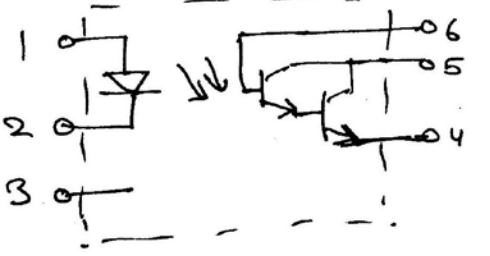
function is reverse biased. For the duration of the negative half cycle of the input Q_1 base emitter function is reversed and Q_2 conducts, pulling the output down to follow the input. Thus, the complementary emitter follower is a large scale circuit with the low output impedance. Another advantage is, this circuit does not require transformer. This saves on weight and cost



b. Draw the circuits of opto-coupler with SCR and Triac and briefly explain these circuits.

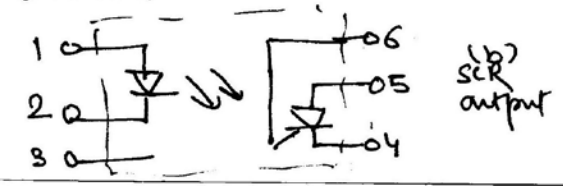
Answer:

(a) Darlington output type : the output stage provides much higher CTR than a BJT photo transistor output stage but it also has slower response time

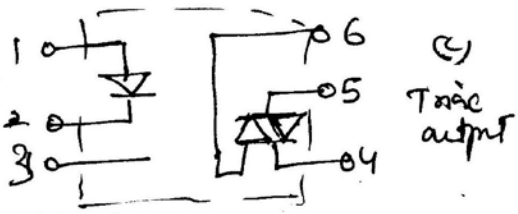


(a) Darlington output

(b) & (c) SCR & triac type are a light activated SCR and light activated triac type. They are used with the kind of control circuits where high electrical isolation between the triggering circuit and the control device is an additional requirement CTR doesn't apply to SCR and Triac output stages instead, the LED current needed to trigger the thyristor is of interest.



(b) SCR output

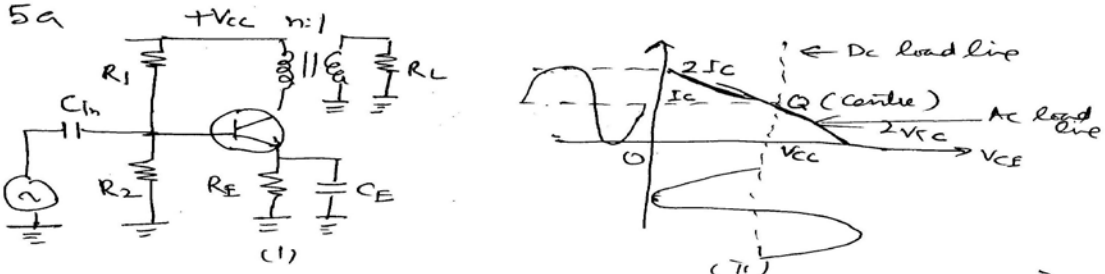


(c) Triac output

c. Show that maximum collector efficiency of class A transformer coupled power amplifier is 50%.

Answer:

5a



ckt (i) shows the transformer coupled class A amplifier under zero signal conditions, the effective resistance in the collector ckt is that of the primary winding of the transformer. The primary resistance has a very small value and is assumed zero. Therefore dc load line is a vertical line rising from V_{cc}. When signal is applied the collector current will vary about the operating point Q. In order to get maximum ac power output, the peak value of collector current due to signal alone should be equal to the zero signal collector current I_C.

During the peak of the positive half cycle of the signal, the total current is $2I_C$ and $V_{ce} = 0$. During the negative peak of the signal, the collector current is zero and $V_{ce} = 2V_{cc}$

∴ Peak to peak collector – emitter voltage is

$$V_{ce(p-p)} = 2V_{cc}$$

peak to peak collector current $i_{c(p-p)} = 2I_C$

$$= \frac{V_{ce(p-p)}}{R'_L} = \frac{2V_{cc}}{R'_L}$$

where R'_L is the reflected value of load R_L and appears in the primary of the transformer if $n (= N_P/N_S)$ is the turns ratio of the transformer then $R'_L = n^2 R_L$

dc power input $P_{dc} = V_{cc} I_C = I_C^2 R'_L$

Max. ac output power $P_{ac(max)} = \frac{V_{ce(p-p)} \times i_{C(p-p)}}{8}$

$$= \frac{2V_{cc} \times 2I_C}{8} = \frac{1}{2} V_{cc} I_C = \frac{1}{2} I_C^2 R'_L$$

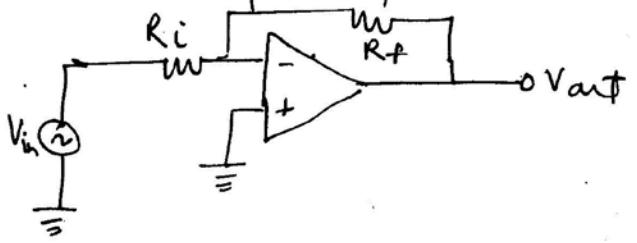
Max collector $\eta = \frac{P_{ac(max)}}{P_{dc}} \times 100 = \frac{(1/2) I_C^2 R'_L}{I_C^2 R'_L} \times 100 = 50\%$

Two BJTs connected ...

Q.6 a. What is the need of negative feedback in OPAMP?

Answer:

6(a) An op-amp is almost always operated with negative feedback i.e. a part of the output is fedback in phase opposition to the input. With negative feedback, the voltage gain can be reduced and controlled so that op-amp can function as linear amplifier. In addition to providing a controlled and stable gain, negative feedback also provides for control of the input and output impedances and amplifier bandwidth



b. Define the following parameter and give their values for IC 723

(i) Input bias current (ii) CMMR

(iii) Output resistance (iv) Input offset voltage

Answer:

(b) (a) The average of the currents entering into (-) input and (+) input terminals of an op-amp. Its value is 500 nA for 741C

(b) CMMR is typically 90 dB.

(c) It is the resistance between the output terminals of the op-amp and the ground. It is 75Ω for the 741C op-amp

(d) It is the voltage that must be applied between the input terminals of an op-amp to nullify the output for 741C, the maximum value is 6mV

c. For the differentiator circuit shown in Fig.4, find:
(i) the expression for the output voltage
(ii) the output voltage for the given input.

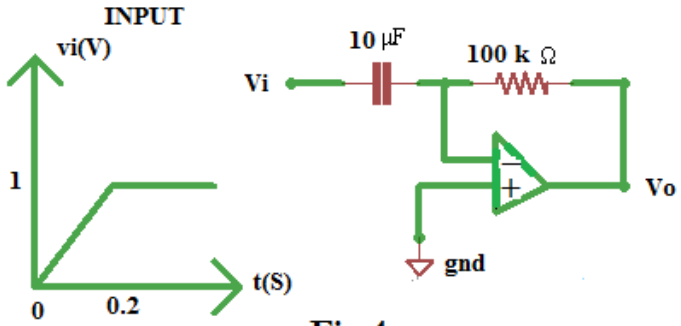


Fig.4

Answer:

current thro R2

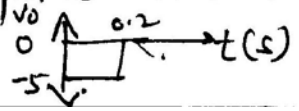
(i) for the differentiator, the output voltage is given by

$$V_o = -R_C \frac{dv_i}{dt} = -(100K\Omega \times 10\,\mu F)\frac{dv_i}{dt}$$

$$= -(100\times10^3\,\Omega)\times(10\times10^{-6}\,F)\frac{dv_i}{dt} = -\frac{dv_i}{dt}$$

(ii) Since the input voltage is straight line between 0 & 0.2sec the output voltage is $V_o = \frac{-dv_i}{dt} = \frac{(1-0)}{0.2} = -5V$

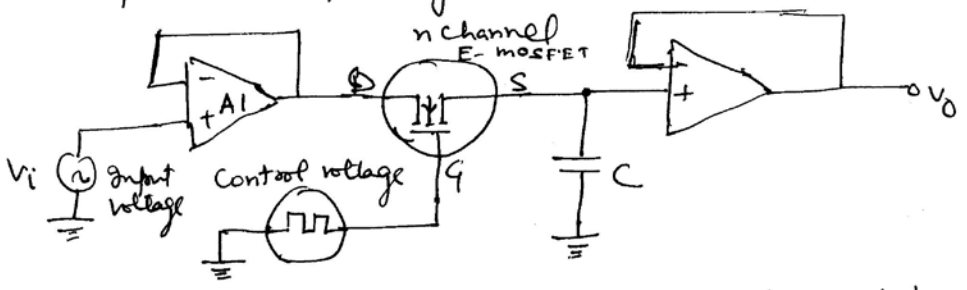
Therefore between 0 to 0.2s the output voltage is constant at −5V for $t > 0.2$ s the input is constant so that output voltage is zero.



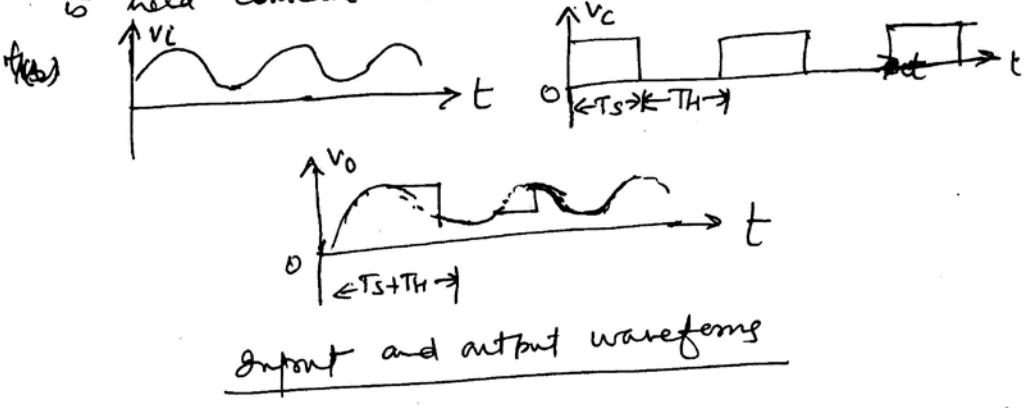
Q.7 a. Draw and explain Sample and Hold circuit using OPAMP. Draw input and output waveform of the circuit.

Answer:

Ans 7(a) A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. The circuit shown in fig



The n channel E-MOSFET works as a switch and is controlled by the control voltage V_c and the capacitor C stores the charge. The analog signal V_i to be sampled is applied to the drain of E-MOSFET and the control voltage V_c is applied to its gate. When V_c is positive the E-MOSFET turns on and the capacitor C charges to the instantaneous value of input V_i with a time constant $[R_o + r_{DS(on)}]C$. Here R_o is the output resistance of the voltage follower A_1 and $r_{DS(on)}$ is the resistance of the MOSFET when on. Thus the input voltage V_i appears across the capacitor C and then at the output through the voltage follower A_2. When V_c is zero the E MOSFET is off. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it. The time period T_H of V_c during which the voltage across the capacitor is held constant is called hold period



Input and output waveforms

b. For the circuit shown in the Fig.5 assuming that the input current is negligible, show that $v_o / v_i = f(R_2, R_1, A)$ and that it may be approximately to $v_o / v_i = -(R_2 / R_1)$.
Explain the purpose of R_3

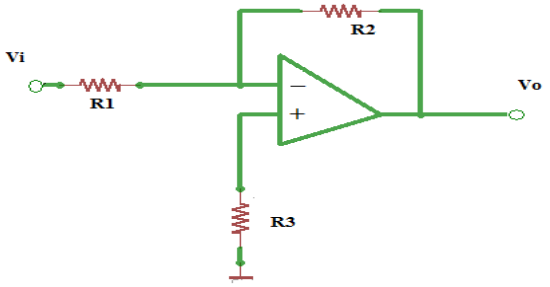


Fig.5

Answer:

7(b) Let the non-inverting input be v_g. current in R_1 be i_1, and the current in R_2 be i_2

$$\therefore i_1 = \frac{v_i - v_g}{R_1} \quad \text{and} \quad i_2 = \frac{v_g - v_o}{R_2}$$

But since amplifier input current is zero $i_1 = i_2$

$$\therefore \frac{v_i - v_g}{R_1} = \frac{v_g - v_o}{R_2}$$

Now $v_o = -A v_g$, where A is the openloop gain

$$\therefore \frac{v_i + \frac{v_o}{A}}{R_1} = -\frac{\left(\frac{v_o}{A} + v_o\right)}{R_2}$$

$$\therefore \frac{v_o}{v_i} = -\frac{R_2}{R_1}\left(\frac{1}{1 + \frac{R_1 + R_2}{A R_1}}\right) \quad \text{for large values of A } \frac{v_o}{v_i} \simeq -\frac{R_2}{R_1}$$

The purpose of R_3 is to reduce the effect of input offset voltage due to input bias current

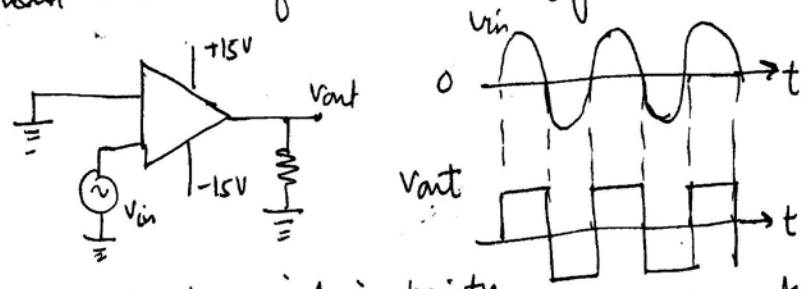
$$\therefore R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

Q.8 a. What are the applications of comparators? Explain the operation of zero crossing detector.

Answer:

8(a) Various important applications of comparator are
(i) Zero crossing detector (ii) Window detector
(iii) Time marker generator (iv) Pulse meter
(v) Level detector (vi) Square wave generator

Zero crossing detector: when one of the input of comparator is connected to ground It is known as Zero crossing detector because output changes when input crosses 0V The circuit and waveform shown in fig



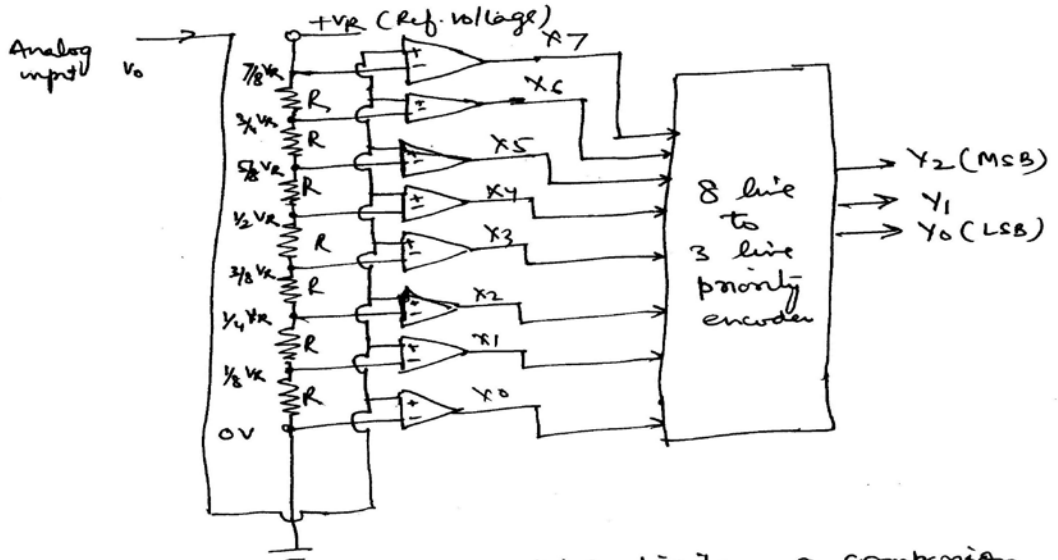
when the input signal is positive going the output is driven to positive maximum value. When the input crosses the zero axis and begins to go negative, the output is driven to negative maximum value

Q.9 Write Short notes on any **TWO** of the following:
(i) 723 general purpose voltage regulator
(ii) Flash type A/D convertor
(iii) IC voltage regulator

Answer:

9(a) Current Boosting. The maximum current that 723 IC regulator can provide is 140 mA. which is not sufficient for many applications and it is possible to boost the current level simply by adding a boost Transistor Q_1 to the voltage regulator. The collector current of the pass transistor Q_1 comes from the Unregulated dc supply The output current from V_o terminal drives the base of the

9 (b) It is the fastest and most expensive type ADC 3 bit A/D converter shown in fig consist of a resistive divider network, 8 op-amp comparators and 8 line to 3 encoder



At each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the ref. voltage V_R and ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially and disadvantage that the number of comparators required almost doubles for each added bit. For large value of n, the more complex is the parity encoder

Text Books

1. Electronic Devices and Circuits, Fourth Edition, David A Bell, PHI (2006).

2. Linear Integrated Circuits, Revised Second Edition, D. Roy Choudhury, Shail B. Jain, New Age International Publishers.